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W-8000 München 26(DE)(54) **Echo canceler having adaptive digital filter unit associated with delta-sigma modulation circuit.**

(57) An echo canceler comprises an adaptive digital filter circuit (42) for producing an echo replica signal on the basis of a transmit digital signal (TD) and a first digital signal indicative of a far-end signal, and an adder (45) for eliminating the echo signal from a received signal with reference to the echo replica

signal, wherein the echo replica signal is modulated by a delta-sigma modulation circuit (43) and, thereafter, converted into an analog signal for allowing the adder to operate on the echo replica signal and the received signal both in an analog form so that the adder with a narrow dynamic range can be available.

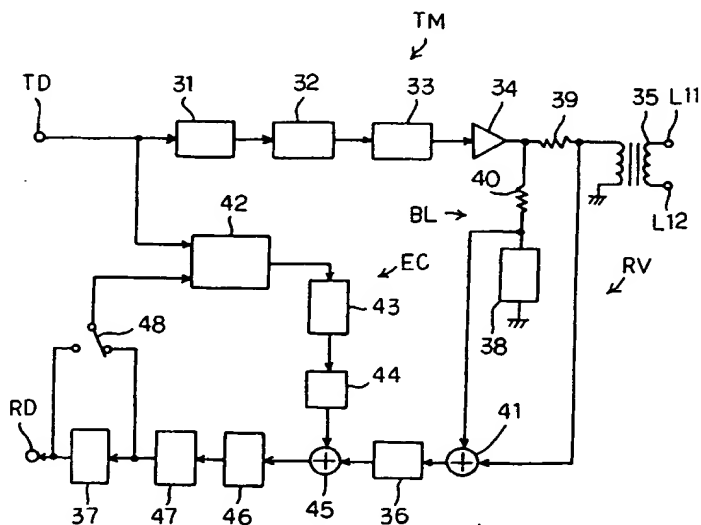


Fig. 3

FIELD OF THE INVENTION

This invention relates to a transceiver for a two-wire digital transmission system, more particularly, to an echo canceler equipped with adaptive digital filter unit.

DESCRIPTION OF THE RELATED ART

An echo canceler carries out echo cancellation on a digital input signal converted through an analog-to-digital conversion by using an echo replica signal produced by an adaptive digital filter unit. Typical examples of the echo cancelers are disclosed in "An ANSI Standard ISDN Transceiver Chip Set", ISSCC '89 Technical Digest, pages 256 and 257; in "An ISDN Echo-Canceling Transceiver Chip for 2B1Q Coded U-Interface", ISSCC '89 Technical Digest, pages 258 and 259; and in "2B1Q Transceiver for the ISDN Subscriber Loop", ISSCC '89 Technical Digest, pages 260 and 261, respectively.

Fig. 1 shows a prior art transceiver with an echo canceler incorporated in a two-wire digital transmission system, and the echo canceler aims at elimination of echo. Referring to Fig. 1, the prior art transceiver largely comprises a signal transmission section TM and an echo canceler EC. In the signal transmission section TM, a delay circuit 1 retards a transmit digital data signal TD, and a digital-to-analog converting circuit 2 converts the transmit digital signal TD to an analog data signal. A low pass filter circuit 3 eliminates high-frequency components from the analog data signal, and the analog data signal is, then, supplied to a line driving circuit 4. The line driving circuit 4 is coupled through a resistive element 5 to a transformer 6, and a two-wire signal path L1 and L2 are further coupled to the transformer 6. Thus, data information is transferred from the transmit digital data signal TD to the analog data signal, and the line driving circuit 5 allows the two-wire signal path L1 and L2 to propagate the data information in cooperation with the transformer 6.

The line driving circuit 4 is further coupled through a resistive element 7 to a balancing network 8, and the transformer 6 and the balancing network 8 are coupled in parallel to two input nodes of an adder 9. If Equation 1 is satisfied, a perfect balancing is achieved, and the adder 9 relays only a received far-end signal to a low pass filter circuit 10.

$$R4/Zb = R3/Z1 \quad \text{Equation 1}$$

R3 and R4 are resistances of the resistive elements 5 and 7, Zb is the impedance of the balancing network 8, and Z1 is the impedance of the two-

wire signal path L1 and L2 and the transformer 6. In the prior art transceiver, the resistive elements 5 and 6, the balancing network 8 and the adder 9 form a hybrid integrated circuit 11.

However, the two-wire signal path L1 and L2 is a distributed constant circuit, and the balancing network is a concentrated constant circuit. Therefore, the perfect balancing is hardly achieved, and the balancing network 8 can not perfectly prevent a received signal RD from an echo due to the data signal indicative of the data information. This is the reason why the echo canceler EC is incorporated in the transceiver. Assuming now that the maximum loss on the two-wire signal path L1 and L2 is 50 dB and that the balancing network 8 decreases the echo by 20 dB, the echo canceler is expected to decrease the echo by 50 dB if targeting the signal/echo ratio for 20 dB.

The echo canceler EC incorporated in the prior art transceiver behaves as follows. The output signal of the adder 9 contains the far-end signal as well as the echo, and high frequency components outside the band are eliminated from the output signal of the adder 9 by means of a low pass filter circuit 10. The output signal of the low pass filter circuit 10 is converted to a digital signal through an analog-to-digital converting circuit 11, and the analog-to-digital converting circuit 11 is usually of the over-sampling type, because a strict linearity is expected. The digital signal thus produced is fed to a digital low pass filter circuit 12, and quantize noises are eliminated from the digital signal. The digital low pass filter circuit 12 further achieves a decimation from the over-sampling frequency to a baud-rate frequency, and the baud-rate frequency is equal to the frequency of the transmit signal. The output signal of the digital low pass filter circuit 12 is supplied to one of the input ports of an adder 13. The transmit digital data signal TD was supplied to an adaptive digital filter circuit 14, and an echo replica signal at the baud-rate is produced by the adaptive digital filter circuit 14. The echo replica signal is fed to the other input port of the adder 13, and the echo signal is eliminated from the output signal of the digital low pass filter circuit 12. In other words, the output signal of the adder 13 contains the far-end signal only. Upon completion of training, a switching circuit 15 is changed from the output of the adder 13 to the output of an equalizer 14 as will be described hereinbelow. The equalizer 14 eliminates the transmission distortion from the output signal or the far-end signal, and produces the received signal RD.

The adaptive digital filter circuit 14 is hereinbelow described in detail with reference to Fig. 2. The adaptive digital filter circuit 14 has two input ports IN1 and IN2 and an output port OUT. The transmit digital data signal TD is supplied to the

input port IN1, and the other input port IN2 is selectively coupled through the switching circuit 15 to the output of the adder 13 and the output of the equalizer 14. While the adaptive digital filter circuit carries out the training operation, the switching circuit 15 allows the output signal of the adder 13 to reach the other input port IN2. However, if the training operation is completed, the switching circuit 15 supplies the far-end signal or the received signal RD to the other output port IN2.

A series combination of delay units each labeled with "T" is coupled to the input port IN1, and each of the delay units introduces a time delay equivalent to a single period of the baud rate into propagation of the transmit digital data signal TD. A plurality of multipliers each labeled with "X" are provided in association with the delay units. The leftmost multiplier multiplies a signal at the input port IN2 by alpha which is a coefficient for controlling a training speed, and the other multipliers respectively multiply the transmit digital data signal TD and the delay signals sequentially delayed by the product of the leftmost multiplier. Alpha is usually much smaller than 1, i.e. $\alpha \ll 1$. The products thus produced by the multipliers are respectively supplied to a plurality of integrators each labeled with "I", and a plurality of multipliers each labeled with "X" multiply the integrals by the transmit signal and the delay signals thereof, respectively. The products thus produced by the second stage of the multipliers are added to one another by an adder labeled with "+". Each series combination of the delay unit, the first-stage multiplier, the integrator and the second-stage multiplier forms a tap.

Assuming now that the signal at the input port IN2 does not contain the far-end signal, an error signal of the echo canceler is fed to the input port IN2. The taps calculate a correlation between the transmit digital data signal and error signal, and integrate at the integrators. As a result, the integrators accumulate the waveform of echo signal sampled at the baud rate, and the waveform of the echo is fed from the taps to the adder in synchronism with the transmit digital data signal. The adder adds the waveforms fed from the taps and produces the echo replica signal. Even if the signal at the input port IN2 contains the far-end signal, the circuit behavior of the adaptive digital filter circuit is similar to the above described sequence, because no correlation is found between the transmit digital data signal and the far-end signal.

As described hereinbefore, the high precision analog-to-digital converting circuit 11 is the indispensable component of the prior art echo canceler, because the characteristics of the prior art echo canceler is dependent upon the linearity of the analog-to-digital converting circuit 11. This re-

sults in a large circuit arrangement of the transceiver. Since the adder 9 is located at the previous stage of the analog-to-digital converting circuit 11, the sum of the echo signal and the far-end signal is supplied to the high-precision analog-to-digital converting circuit 11, and the digital signal tends to be constituted by a long bit string. This means that the adder 13 needs a wide dynamic range for adding the echo replica signal to the output signal of the digital low pass filter circuit 12, and the adder 13 with a wide dynamic range makes the circuit arrangement of the transceiver large in size.

If the echo replica signal is converted into an analog signal and the analog echo replica signal is shaped by a low pass filter circuit, the echo signal may be deleted from the analog output signal of the adder 9 through a subtraction of the analog replica signal prior to the digital-to-analog conversion. However, this approach also needs a high precision analog-to-digital converting circuit with a strict linearity as well as a high performance low pass filter circuit, and is less feasible.

SUMMARY OF THE INVENTION

It is therefore an important object of the present invention to provide an echo canceler which is smaller in circuit arrangement than the prior art echo canceler.

To accomplish the object, the present invention proposes to apply a delta-sigma modulation technique to an echo replica signal.

In accordance with the present invention, there is provided an echo canceler associated with a signal transmission unit for transmitting a transmit digital signal and operative to eliminate an echo signal from a received analog signal containing at least the echo signal and a far-end signal, comprising: a) an adaptive digital filter circuit supplied with the transmit digital signal and a first digital signal without the echo signal so as to see a correlation therebetween, and operative to produce a digital echo replica signal; b) a delta-sigma modulation circuit operative to carry out a delta-sigma modulation on the digital echo replica signal and producing a second digital signal representative of the digital echo replica signal; c) a digital-to-analog converting circuit for converting the second digital signal to a first analog signal; d) a first adder supplied with the received analog signal and the first analog signal, and operative to eliminate the echo signal from the received analog signal for producing a received analog signal without the echo signal; and e) means operative to carry out a delta-sigma analog-to-digital converting operation on the received analog signal without the echo signal, and producing the first digital signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the echo canceler according to the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which:

Fig. 1 is a block diagram showing the circuit arrangement of the prior art transceiver;

Fig. 2 is a block diagram showing the circuit arrangement of an adaptive digital filter circuit incorporated in the prior art transceiver;

Fig. 3 is a block diagram showing the circuit arrangement of a transceiver equipped with an echo canceler according to the present invention;

Fig. 4 is a block diagram showing the arrangement of an adaptive digital filter circuit incorporated in the transceiver shown in Fig. 3;

Fig. 5 is a block diagram showing the arrangement of a second order delta-sigma modulation circuit incorporated in the transceiver shown in Fig. 3;

Figs. 6A and 6B are graphs each showing residual echo in terms of time;

Fig. 7 is a circuit diagram showing the arrangement of a combined circuit of a digital-to-analog convertor and an adder incorporated in another transceiver according to the present invention;

Fig. 8 is a diagram showing the waveforms of clock signals different in phase and used in the combined circuit shown in Fig. 7;

Fig. 9 is a circuit diagram showing the arrangement of a balance circuit according to the present invention;

Fig. 10 is a circuit diagram showing the arrangement of another combined circuit of a digital-to-analog convertor and an adder incorporated in still another transceiver according to the present invention;

Fig. 11 is a diagram showing the waveforms of clock signals different in phase from each other and used in the combined circuit shown in Fig. 10;

Fig. 12 is a circuit diagram showing the arrangement of a balance circuit according to the present invention;

Fig. 13 is a block diagram showing the arrangement of another second order delta-sigma modulation circuit incorporated in still another transceiver according to the present invention; and

Figs. 14A and 14B are graphs each showing residual echo in terms of time.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

Referring to Fig. 3 of the drawings, a transceiver according to the present invention largely comprises a signal transmission section TM, and a signal receiving section RV. The signal transmission section TM is similar in circuit arrangement to that of the prior art transceiver, and comprises a delay circuit 31, a digital-to-analog converting circuit 32, a low pass filter circuit 33 and a line driving circuit 34. A transformer is shared between the signal transmission section TM and the signal receiving section RV, and is coupled to a two-wire data signal path L11 and L12. A transmit digital data signal TD indicative of data information is supplied to the delay circuit 31, and the signal transmission section TM drives the transformer 35 for producing an analog data signal carrying the data information. Then, the two-wire data signal path L1 and L2 propagates the analog data signal to a destination as similar to the signal transmission section TM of the prior art transceiver.

The signal receiving section RV largely comprises a balancing circuit BL, an echo canceler EC, a low pass filter circuit 36 coupled between the balancing circuit BL and the echo canceler EC, and an equalizer 37 coupled to the echo canceler EC. The balancing circuit BL comprises a balancing network 38, a resistive element 39 coupled between the line driving circuit 34 and the transformer 35, a resistive element 40 coupled between the line driving circuit 34 and the balancing network 38, and an adder 41. However, the balancing circuit BL, the low pass filter circuit 36 and the equalizer 37 are similar to those of the prior art transceiver, and no further description is incorporated hereinbelow.

The echo canceler EC comprises an adaptive digital filter circuit 42 supplied with the transmit digital data signal TD, a second order delta-sigma modulation circuit 43 coupled to the output port of the adaptive digital filter circuit 42, a digital-to-analog converting circuit 44 coupled to the second order delta-sigma modulation circuit 43, an adder 45 coupled to the digital-to-analog converting circuit 44 and the low pass filter circuit 36, a second order delta-sigma analog-to-digital converting circuit 46 coupled to the adder 45, a digital low pass filter circuit 47 coupled to the second order delta-sigma analog-to-digital converting circuit 46, and a switching circuit 48 for selectively coupling the digital low pass filter circuit 47 and the equalizer 37 to the adaptive digital filter circuit 42. The adaptive digital filter circuit 41 and the digital low pass filter circuit 46 respectively correspond to the adaptive digital filter circuit 14 and the digital low pass filter circuit 12, and achieve the similar tasks, respectively.

The adaptive digital filter circuit 42 produces an echo replica signal at the baud rate frequency,

and the echo replica signal is supplied to the second order delta-sigma modulation circuit 43. The echo replica signal is sampled at an over-sampling frequency n times larger than the baud rate frequency where n is an integer, and is, thereafter, modulated in a second order delta-sigma modulating manner. The second order delta-sigma modulation circuit 43 produces a single bit digital signal at the over-sampling frequency, and the digital-to-analog converting circuit 44 converts the single bit digital signal to an analog signal indicative of either binary number. In this instance, the single bit digital signal and the first analog signal serve as a second digital signal and a first analog signal, respectively. The single bit digital signal and, accordingly, the analog signal converted therefrom are representative of the echo replica signal. On the other hand, the output signal of the balancing circuit BL is fed from the adder 41 to the low pass filter circuit 36, and high frequency components outside of the band is eliminated from the output signal of the balancing circuit BL. The low pass filter circuit 36 supplies the output signal to the adder 45, and the output signal contains a far-end signal and an echo signal. The adder 45 carries out an adding operation on the analog signal representative of the echo replica signal and the output signal containing the far-end signal and the echo signal, and the echo signal is eliminated from the output signal. The output signal indicative of the calculation result is supplied from the adder 45 to the second order delta-sigma analog-to-digital converting circuit 46, and the second order delta-sigma analog-to-digital converting circuit 46 produces a single bit digital signal which serves as a third digital signal. The single bit digital signal is fed to the digital low pass filter 47, and the digital low pass filter circuit 47 eliminates high frequency quantize noise therefrom as well as decimates from the over-sampling frequency to the baud rate frequency. While the adaptive digital filter circuit 42 is in the training, the output signal of the digital low pass filter circuit 47 returns to the adaptive digital filter circuit 42. The output signal of the digital low pass filter circuit 47 does not contain the echo signal, and serves as a first digital signal. The output signal of the digital low pass filter circuit 47 is further fed to the equalizer 37 so that distortion is eliminated for producing a received signal RD.

Turning to Fig. 4 of the drawings, the adaptive digital filter circuit 42 has two input ports IN11 and IN12 and a single output port OUT coupled to the second order delta-sigma modulation circuit 42. The transmit digital data signal TD is supplied to the input port IN11, and the other input port IN12 is coupled to the switching circuit 48. The input port IN11 is coupled to a series combination 42a of time delay circuits T, and each of the time delay circuits

T introduces a unit delay to the transmit digital data signal TD. While the adaptive digital filter circuit 42 is in the training, the output signal without the echo signal is supplied to the input port IN12, and a multiplier 42b multiplies the output signal by the constant alpha. The product is supplied in parallel from the multiplier 42b to a first multiplier array 42c, and the multipliers X of the first array 42c respectively multiply the delayed digital signals fed from the second to last time delay units T by the product of the multiplier 42b. The products of the multipliers X of the array 42c are fed to integrator array 42d, and the integrals are multiplied at a second multiplier array 42e again. The transmit digital data signal TD and the delayed digital signals are supplied to the multipliers X of the second array 42e, and are multiplied by the integrals, respectively. The products of the second multiplier array 42e are totaled at an adder 42f, and the echo replica signal takes place at the output port of the adder 42f.

The adaptive digital filter circuit 42 is slightly modified from the adaptive digital filter circuit 14 of the prior art transceiver. Namely, the first multiplier array 42c to the second multiplier array 42e are offset from the series combination 42a of the time delay circuits T in the right direction of Fig. 4, and the transmit digital data signal TD is supplied to the second multiplier array 42e at later timings rather than the prior art adaptive digital filter circuit. This is because of the fact that the adder 45 is located at the previous stage of the second order delta-sigma converting circuit 46.

Turning to Fig. 5, the second order delta-sigma modulation circuit 43 comprises a first adder 43a supplied with the echo replica signal and a feed-back signal from a time delay unit 43b, a first integrator 43c coupled to the first adder 43a, a second adder 43d coupled to the first integrator 43c and the time delay unit 43b, a second integrator 43e coupled to the second adder 43d, and a quantizer 43f coupled to the second integrator 43e. The single bit digital signal indicative of the echo replica signal takes place at the output port of the quantizer 43f, and is fed to the time delay unit 43b as well as the digital-to-analog converting circuit 44. The adders 43a and 43d, the integrators 43c and 43e, the quantizer 43f and the time delay unit 43b achieve the respective tasks at the over-sampling frequency.

If analog-to-digital converting circuits both inferior in linearity are respectively incorporated in the prior art echo canceler and the echo canceler EC, residual echoes are left in the received digital signals. However, the echo canceler EC according to the present invention is less affectable by poor linearity of the analog-to-digital converting circuit 46. In order to confirm the advantage of the

present invention, a simulation is carried out, and Figs. 6A and 6B illustrate time dependency of the residual echoes simulated for the prior art echo canceler (Fig. 6A) and the echo canceler of the first embodiment (Fig. 6B). The analog-to-digital converting circuits 11 and 46 are modeled by applying 5 % distortion to switched capacitor integrators incorporated in the analog-to-digital converting circuits 11 and 46. Comparing Fig. 6A with Fig. 6B, the residual echo of the first embodiment is decreased to less than -70 dB; however, the prior art echo canceler can decrease the residual echo around -60 dB. This means that the analog-to-digital converting circuit incorporated in the first embodiment is less affectable by poor linearity, and a relatively narrow dynamic range decreases the component circuit elements of the analog-to-digital converting circuit.

As will be understood from the foregoing description, the echo canceler according to the present invention eliminates the echo signal before the analog-to-digital conversion, and, for this reason, the digital circuits 46, 47 and 37 are less affectable by undesirable poor linearity. This results in a narrower dynamic range rather than the prior art echo canceler, and the circuit components are decreased.

Second Embodiment

Turning to Fig. 7 of the drawings, a combined circuit of a digital-to-analog convertor and an adder is implemented by a switched capacitor filter. The digital-to-analog convertor and the adder correspond to the digital-to-analog converting circuit 44 and the adder 45, respectively. The other component circuits of the second embodiment are similar to those of the first embodiment, and, for this reason, no further description on the other component circuits is incorporated hereinbelow.

The combined circuit comprises a single operational amplifier circuit 61, and the non-inverted input node of the operational amplifier circuit 61 is grounded. On the other hand, the inverted input node of the operational amplifier circuit 61 is coupled in parallel to capacitors C1 and C2 through respective switching elements S1 and S2, and the first electrodes of the capacitors C1 and C2 can be grounded through switching elements S3 and S4. The second electrode of the capacitor C1 is selectively coupled to an input node IN21 and a ground node through switching elements S5 and S6, and the second electrodes of the capacitor C2 is selectively coupled to a source of positive reference voltage +Vr, a source of negative reference voltage -Vr and the ground node through switching elements S7, S8 and S9. Between the inverted input node and the output node of the operational

amplifier circuit 61, capacitors C3 and C4 are coupled in parallel, and only the capacitor C3 is associated with switching elements S10, S11, S12 and S13. Namely, the capacitor C4 is directly coupled between the inverted node and the output node, however, the capacitor C3 is coupled through the switching elements S10 and S11. The capacitor C3 can be grounded through the switching elements S12 and S13.

The switching elements are shifted between on-state and off-state with first and second clock signals P1 and P2 as well as with auxiliary clock signals P1h and P1l of the first clock signal P1. The auxiliary clock signals P1h and P1l are produced by a clock generator 62 which comprises two AND gates 62a and 62b and an inverting circuit 62c. An input node IN22 is coupled to the AND gate 62a and the inverting circuit 62c, and the input nodes IN21 and IN22 are coupled to the low pass filter circuit 36 and the second order delta-sigma modulation circuit 43, respectively.

The waveforms of the first and second clock signals P1 and P2 are shown in Fig. 8, and the second clock signal P2 goes up to the high level while the first clock signal P1 remains low. The switching elements S1 to S13 are controlled with the clock signals P1, P2, P1h and P1l, and the capacitor C2, the switching elements S2, S4, S7, S8 and S9 and the clock generator 62 serves as a single bit digital-to-analog convertor. The combined circuit thus arranged achieves the digital-to-analog conversion and an adding operation. Since the digital-to-analog conversion and the adding operation is achieved with only one operational amplifier circuit 61, the circuit arrangement of the second embodiment is simpler rather than the first embodiment.

In the above mentioned circuit, the 1-bit digital-to-analog converting circuit and the adder is implemented by an unbalance switched capacitor circuit. However, if a fully differential operational amplifier is used, it is possible to fabricate a balance circuit. Fig. 9 shows an example of the balance circuit in which single bit digital-to-analog converting circuits and an adder are implemented by a fully differential switched capacitor circuit associated with a fully differential operational amplifier 901. P1 and P2 are clock signals different in phase, and controlling signals P1h and P1l are produced from the clock signal P1 and a system clock signal CLK. In this instance, a differential input IN(+) and IN(-) is supplied to the two 1-bit digital-to-analog converting circuits. The two 1-bit digital-to-analog converting circuits operate on the differential input IN(+) and IN(-), and carry out adding thereon. The balance circuit thus arranged is less sensitive to common mode noises.

Third Embodiment

Fig. 10 illustrates another combined circuit of a digital-to-analog convertor and an adder incorporated in still another transceiver embodying the present invention. The component circuits of the first embodiment except for the digital-to-analog converting circuit 44 and the adder 45 are incorporated in the third embodiment, and the corresponding circuits are labeled with the same references.

The combined circuit comprises two operational amplifier circuits 91 and 92 associated with capacitors C11 to C17 which in turn are associated with switching elements S21 to S43. The non-inverted input nodes of the operational amplifier circuits 91 and 92 are grounded, and the output node of the operational amplifier circuit 92 is coupled to a comparator 93. The capacitors C14 and C17 are directly coupled between the output node and the inverted input node of the operational amplifier circuit 91 and between the output node and the inverted input node of the operational amplifier circuit 92, respectively, and the other capacitors are selectively coupled to an input node IN31, a source of positive reference voltage $+V_r$, a source of negative reference voltage $-V_r$, the operational amplifier circuits 91 and 92 and a ground node.

The combined circuit further comprises a clock generator 94 for producing auxiliary clock signals Pc and Pd, and a controller 95 coupled to the output node of the comparator 93 for producing other auxiliary clock signals Pa and Pb. The clock generator 94 comprises two AND gates 94a and 94b and an inverting circuit 94c, and an input node IN32 is coupled to the AND gate 94a and the inverting circuit 94c. The input nodes IN31 and IN32 are coupled to the low pass filter circuit 36 and the second order delta-sigma modulation circuit 43, respectively.

The waveforms of first and second clock signals P11 and P12 are shown in Fig. 11, and the second clock signal P12 goes up to the high level while the first clock signal P11 remains low. For this reason, the switching elements such as S21 and S23 alternatively turn on and off, and the combined circuit is of the type having the second order delta-sigma analog-to-digital converting circuit 46 and further achieving functions of a digital-to-analog convertor and an adder. The switching elements S30 to S34 and the capacitor C13 serves as a single bit digital-to-analog convertor, and the first integrator of the second order delta-sigma analog-to-digital converting circuit 46 achieves the adding operation. Thus, the combined circuit shown in Fig. 10 deletes operational amplifier circuits from the digital-to-analog converting circuit 44 and the adder 45, and, for this reason, the compo-

nent elements are minimized.

In the above described circuit, the 1-bit digital-to-analog converting circuit, the adder and the second order delta-sigma modulator are implemented by an unbalance switched capacitor circuit. However, it is possible to fabricate a balance circuit as similar to the second embodiment. Namely, Fig. 12 shows the circuit arrangement of a balance circuit where a fully differential second order delta-sigma modulator is coupled to a differential digital-to-analog converting circuit. This balance circuit is less sensitive to common mode noises as similar to the balance circuit shown in Fig. 9.

Fourth Embodiment

Fig. 13 shows the arrangement of another second order delta-sigma modulation 98 circuit incorporated in still another transceiver embodying the present invention. However, the other component circuits are similar to those of the first embodiment, and detailed description is focused upon the second order delta-sigma modulation circuit 98 only. The second order delta-sigma modulation circuit 98 comprises a digital low pass filter circuit 98a and a second order delta-sigma modulation circuit similar to that of the first embodiment. The digital low pass filter circuit 98a is operative at the over-sampling frequency, and carries out an interpolation on the echo replica signal at the baud rate frequency fed from the adaptive digital filter circuit 42. With the digital low pass filter, the echo canceler is improved in the echo restriction characteristics between the sampling points at the baud rate frequency.

In detail, Figs. 14A and 14B shows residual echoes in the received digital signals produced by the first embodiment (Fig. 14A) and the fourth embodiment (Fig. 14B) upon completion of training. The digital low pass filter circuit 98a is implemented by an FIR filter with 96 taps. The vertical strips of Figs. 14A and 14B are matched with the sampling points at the baud rate frequency, and the echo cancelers according to the present invention decrease residual echo to about zero at the sampling points. However, the residual echo between the sampling points depends on the interpolation characteristics. Comparing Fig. 14A with Fig. 14B, the fourth embodiment restricts the residual echo between the sampling points rather than the first embodiment. Thus, the fourth embodiment is improved in the interpolation characteristics by virtue of the digital low pass filter circuit, and can restrict the residual echo due to phase shift of received clock signal. This results in improvement in timing extraction.

Although particular embodiments of the present invention have been shown and described, it will be

obvious to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the present invention.

Claims

1. An echo canceler associated with a signal transmission unit (TM) for transmitting a transmit digital signal (TD) and operative to eliminate an echo signal from a received signal containing at least said echo signal and a far-end signal, comprising:
 - a) an adaptive digital filter circuit (42) supplied with said transmit digital signal and a first digital signal without said echo signal so as to see a correlation therebetween, and operative to produce an echo replica signal; and
 - b) a first adder (45) for eliminating said echo signal from said received signal with reference to said echo replica signal, characterized by
 - c) a delta-sigma modulation circuit (43;98) operative to carry out a delta-sigma modulation on said echo replica signal in a digital form and producing a second digital signal representative of said echo replica signal;
 - d) a digital-to-analog converting circuit (44) for converting said second digital signal to a first analog signal indicative of said echo replica signal, said first analog signal being fed to said adder for allowing said adder to operate on said received signal in an analog form; and
 - e) means (46/47) supplied with said received signal without said echo signal from said adder, and operative to carry out a delta-sigma analog-to-digital converting operation on said received signal without said echo signal, and producing said first digital signal.
2. An echo canceler as set forth in claim 1, in which said delta-sigma modulation circuit (42) is of a second order type, and in which said digital echo replica signal is sampled at an over-sampling frequency n times larger than a baud rate frequency of said transmit digital signal where n is an integer.
3. An echo canceler as set forth in claim 2, in which said means comprise e-1) a second order delta-sigma analog-to-digital converting circuit (46) supplied with said received signal and producing a third digital signal, and e-2) a digital low pass filter circuit (47) for eliminating noises and decimating from said over-sampling

frequency to said baud rate frequency for producing said first digital signal.

4. An echo canceler as set forth in claim 3, in which said echo canceler further comprises f) an equalizer coupled to said digital low pass filter circuit and eliminating a distortion therefrom for producing a received digital signal representative of said far-end signal, and g) a switching circuit selectively coupling said digital low pass filter circuit and said equalizer to said adaptive digital filter circuit.
5. An echo canceler as set forth in claim 4, in which said transmission unit drives a transformer (35) coupled to a two-wire signal path (L11/L12), and in which a balancing circuit (BL) is coupled to said transformer for supplying said received analog signal through a low pass filter circuit (36) to said first adder.
6. An echo canceler as set forth in claim 1, in which said delta-sigma modulation circuit (98) comprises a digital low pass filter (98a) for carrying out an interpolation on said echo replica signal, and a delta-sigma modulator (98b) coupled to said digital low pass filter and carrying out a delta-sigma modulation on an echo replica signal fed from said digital low pass filter.

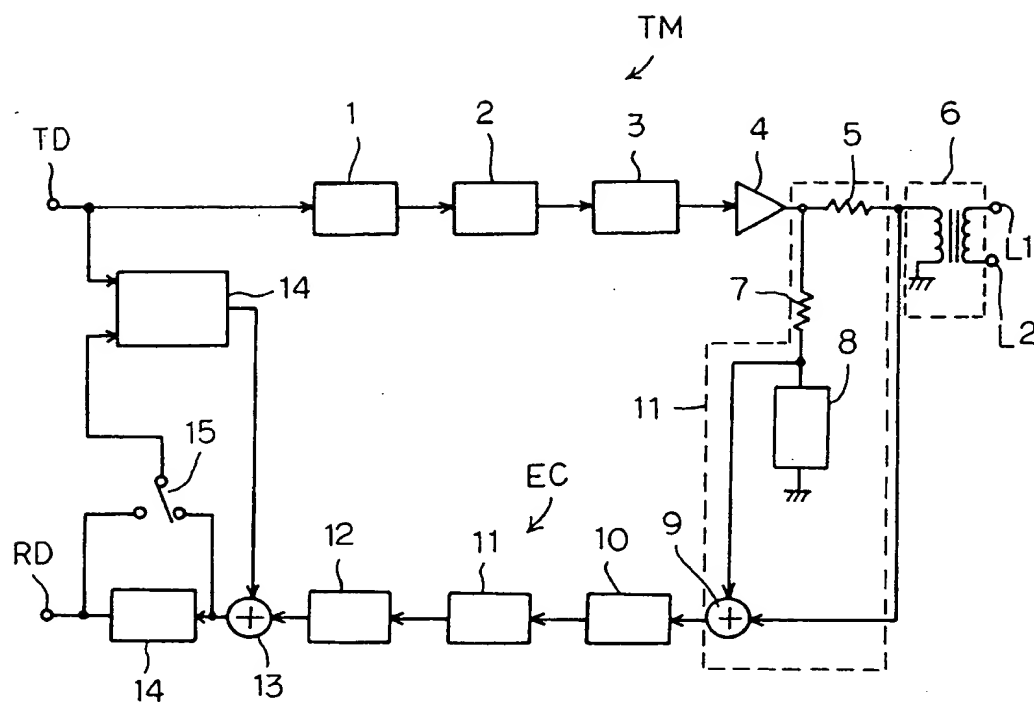


Fig. 1
PRIOR ART

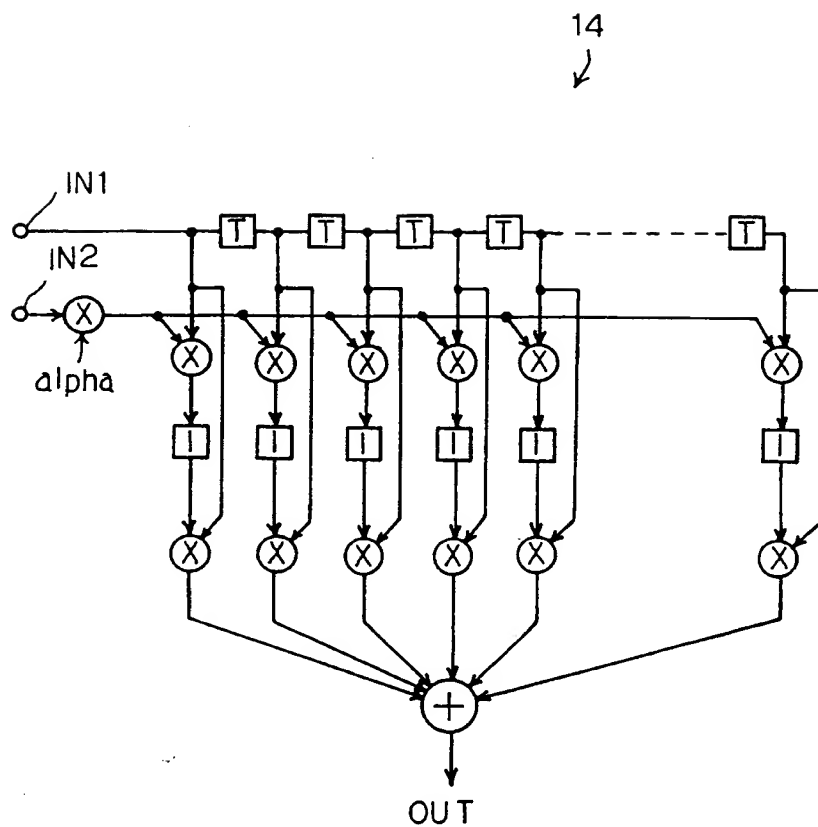


Fig. 2
PRIOR ART

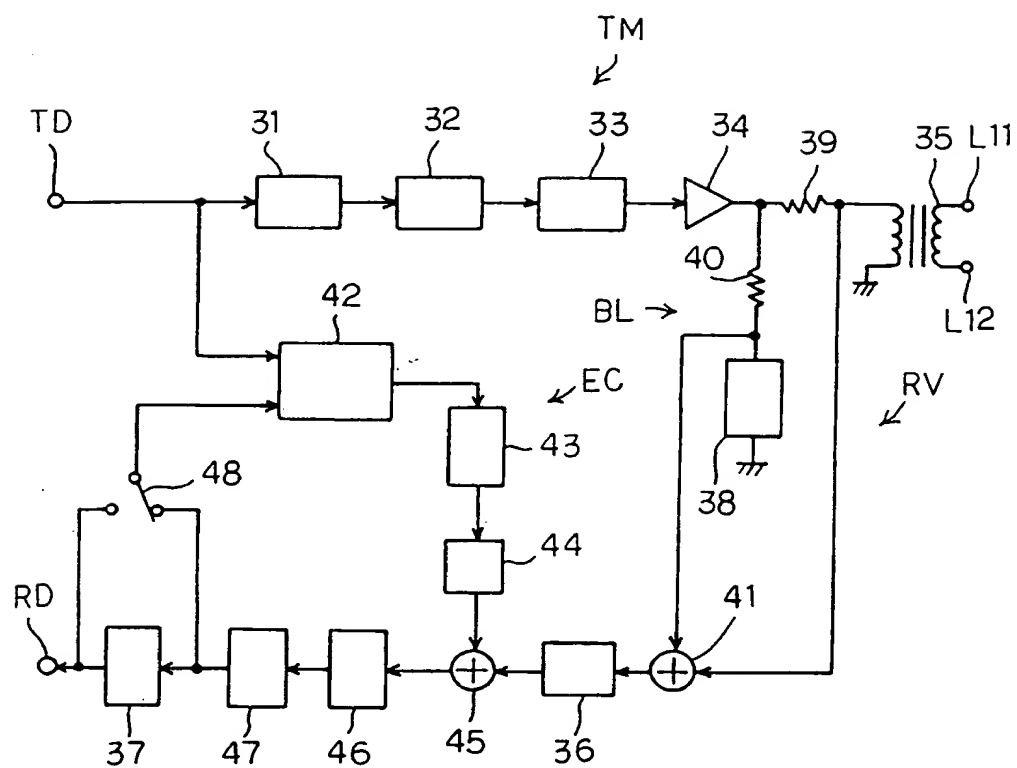


Fig. 3

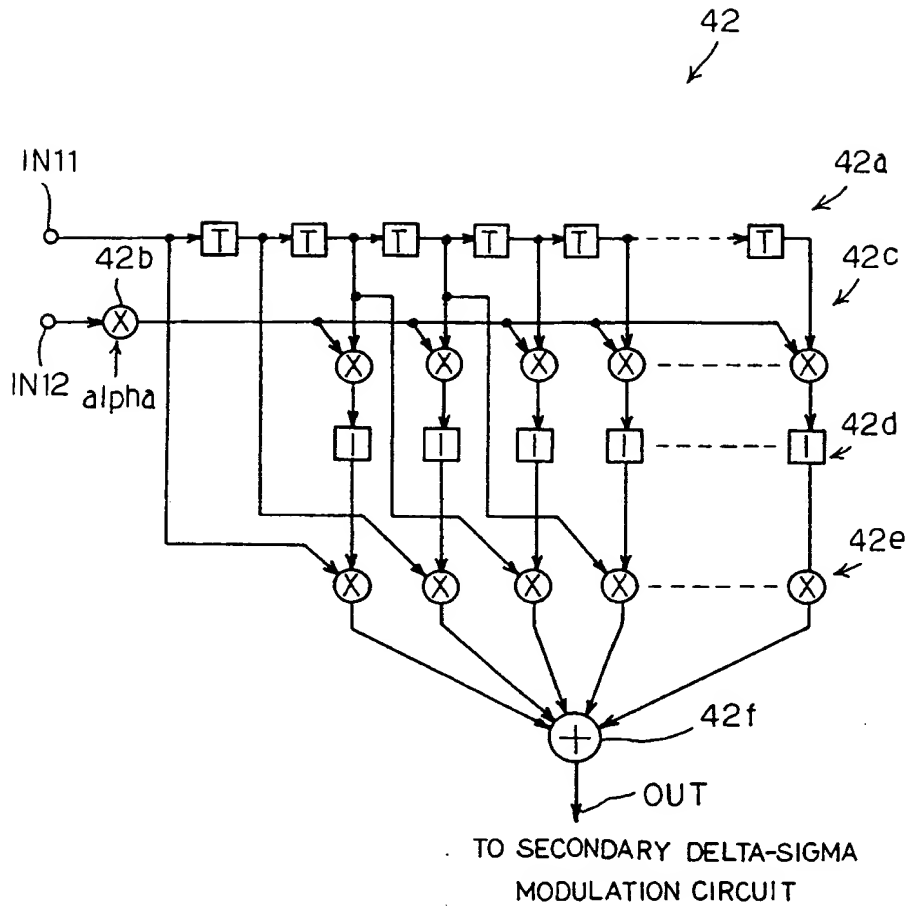


Fig. 4

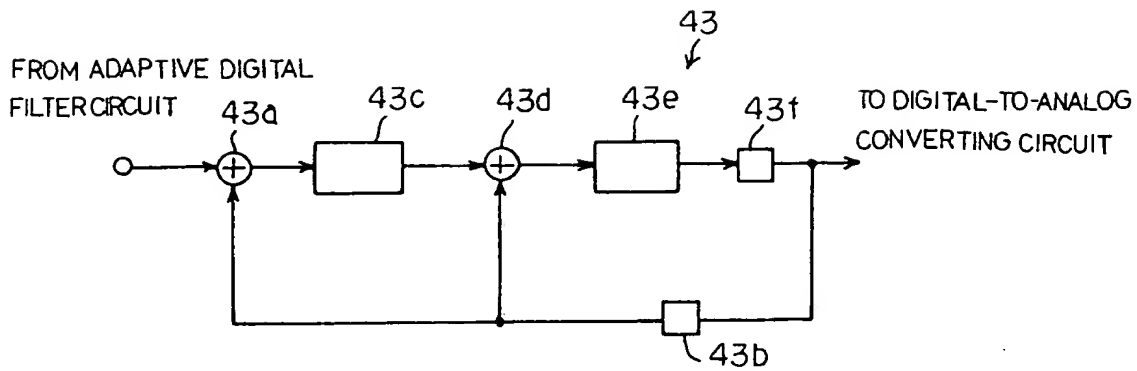


Fig. 5

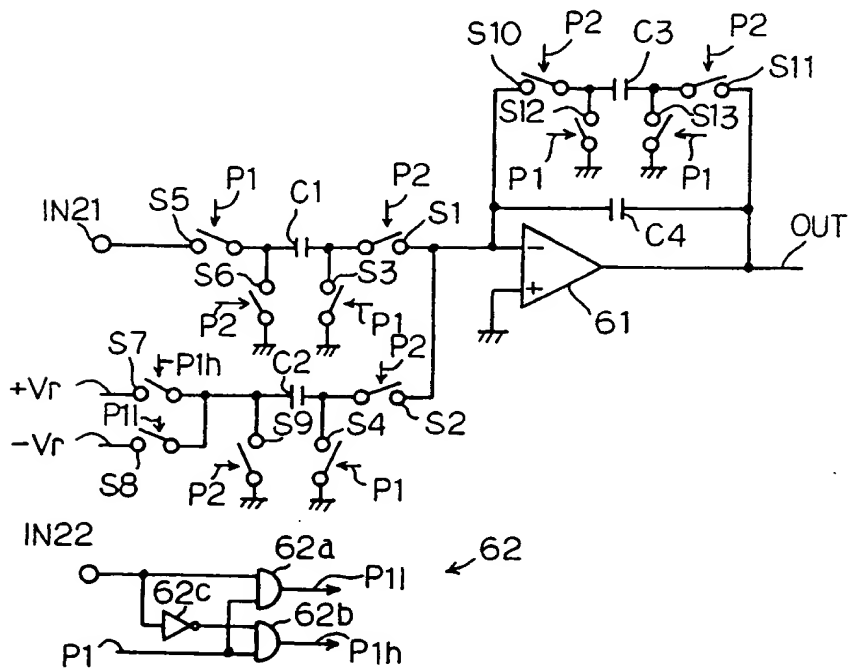


Fig. 7

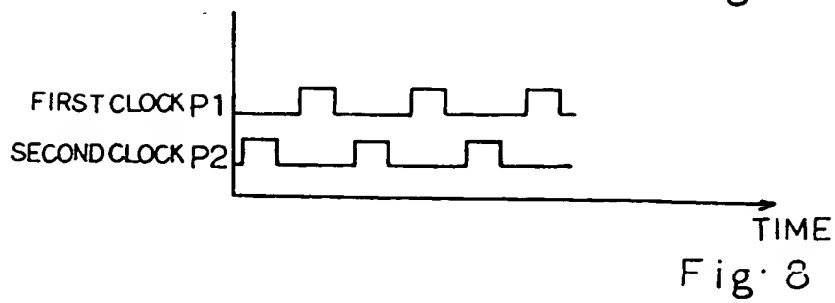


Fig. 8

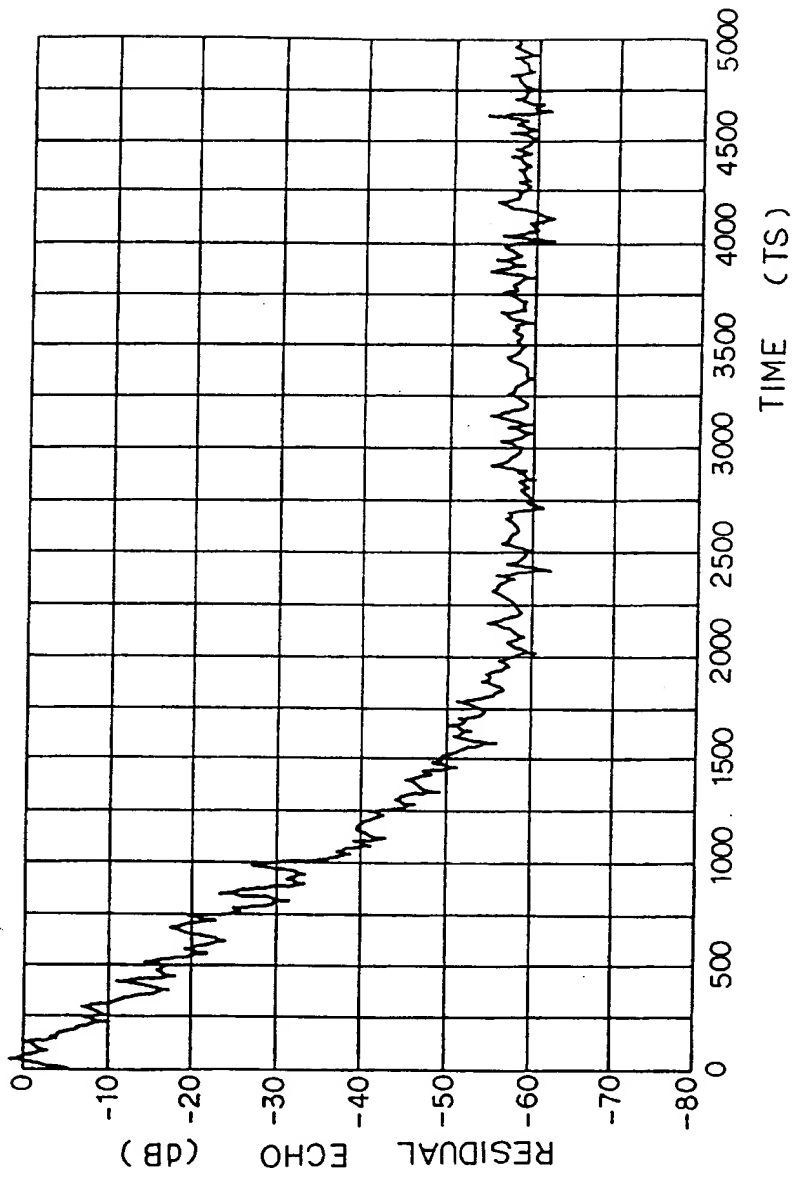


Fig. 6A

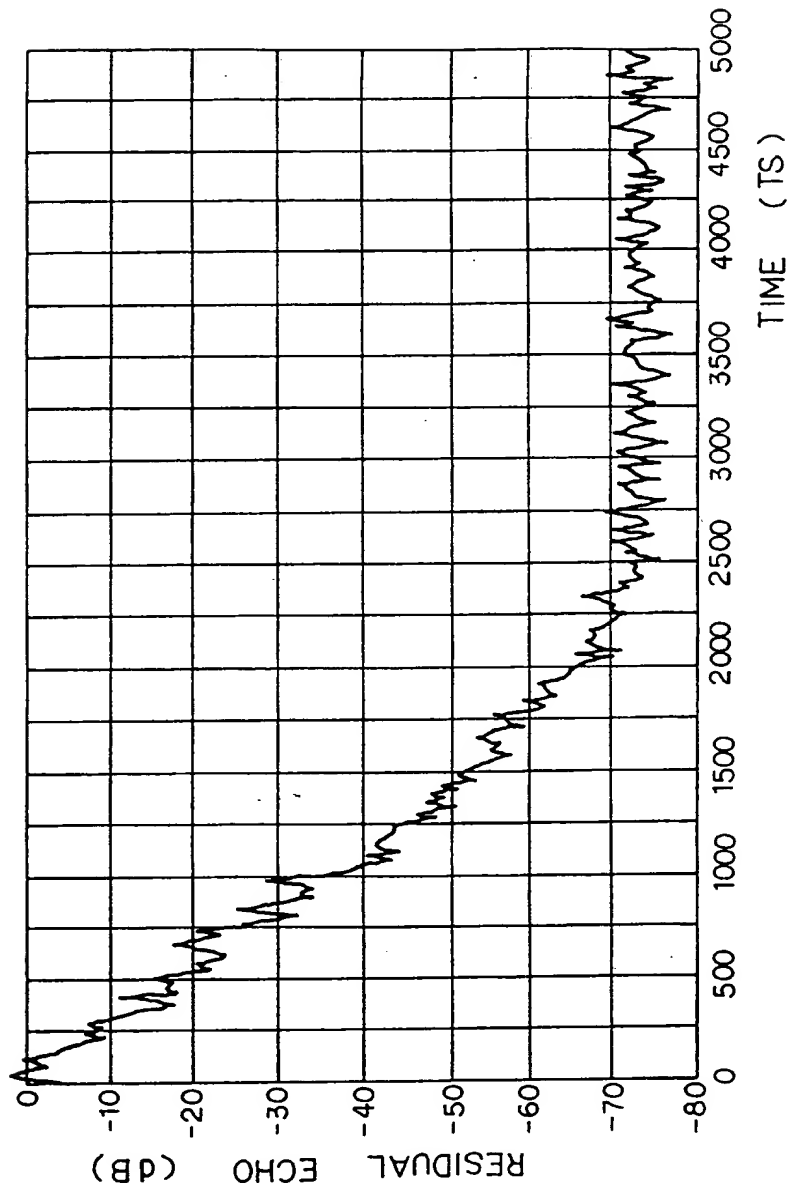


Fig. 6B

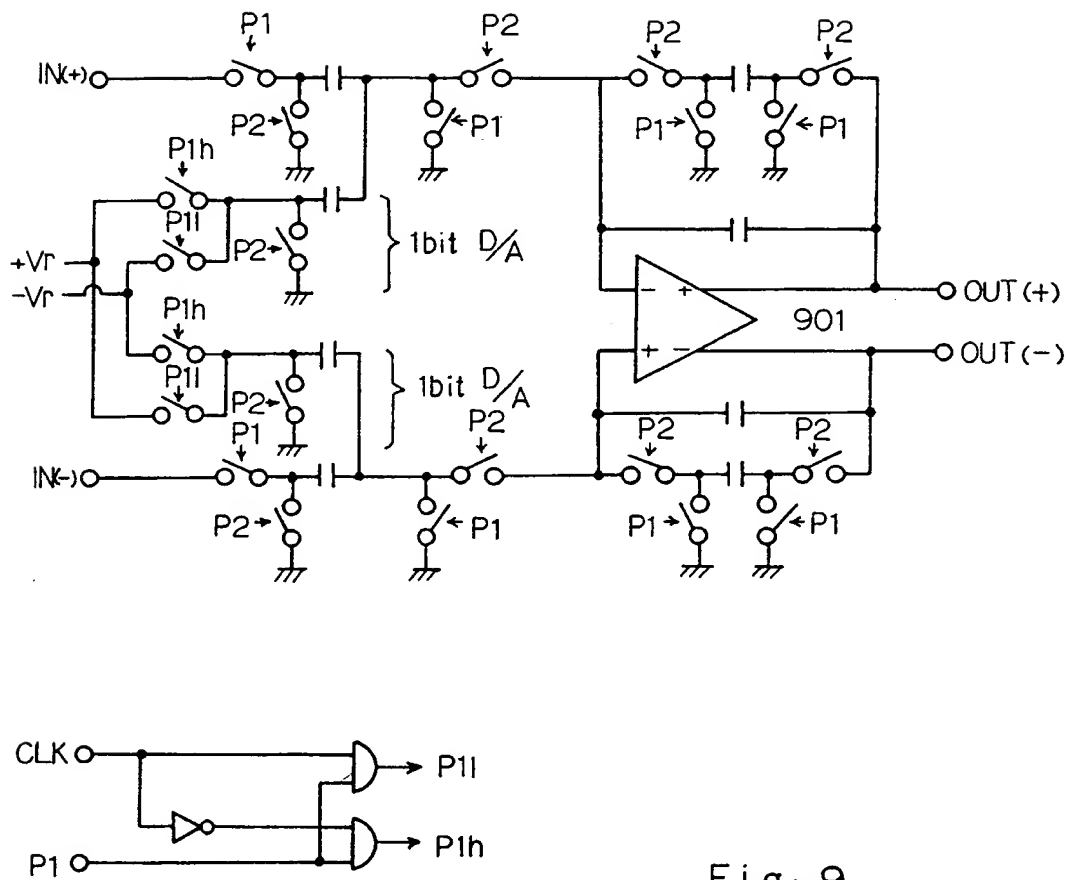


Fig. 9

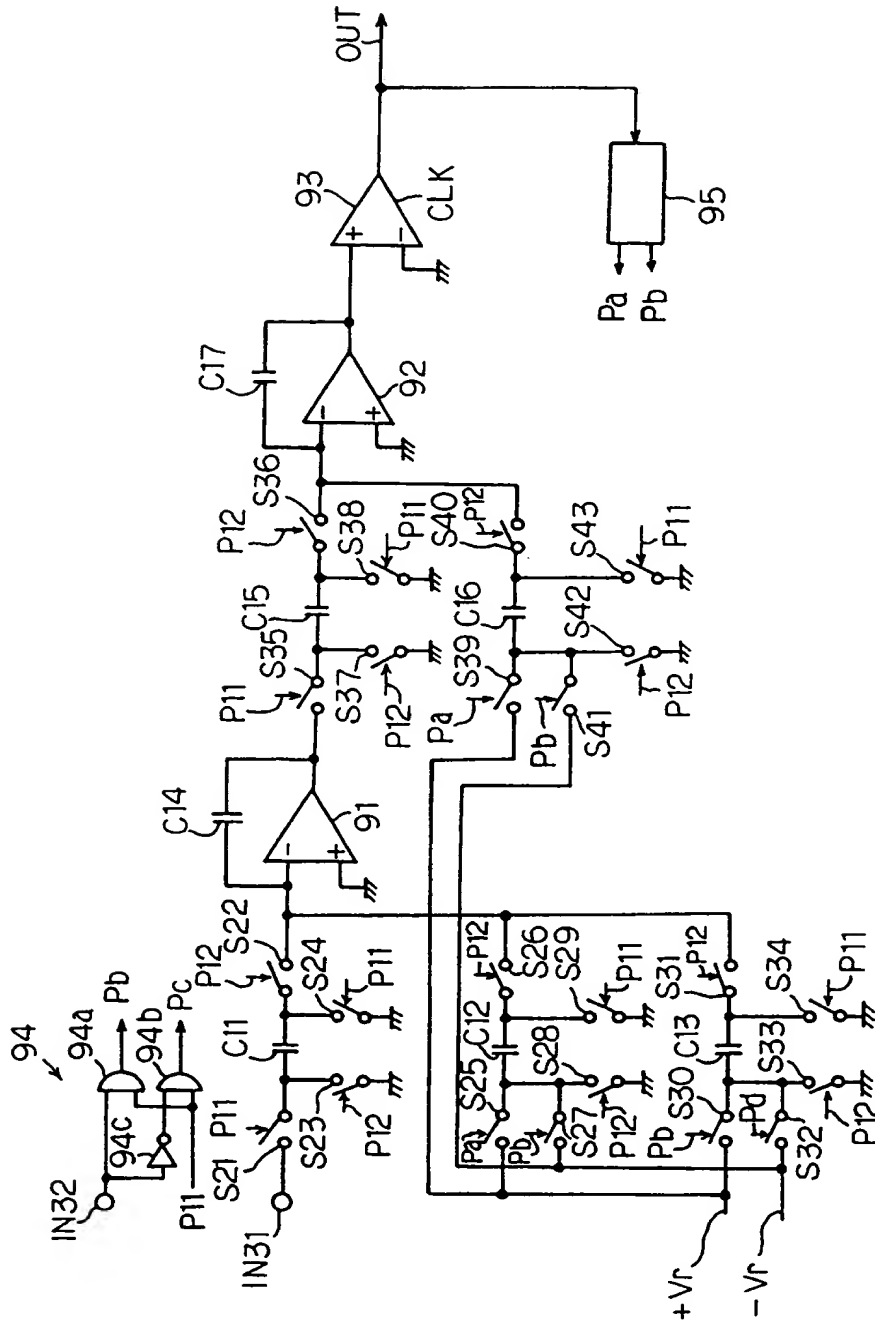


Fig. 10

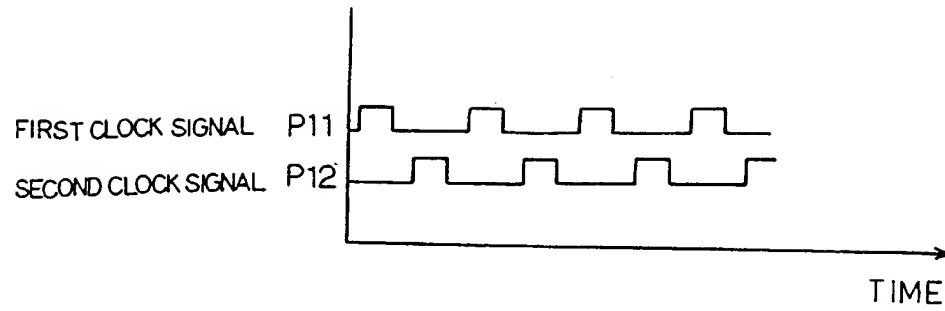


Fig. 11

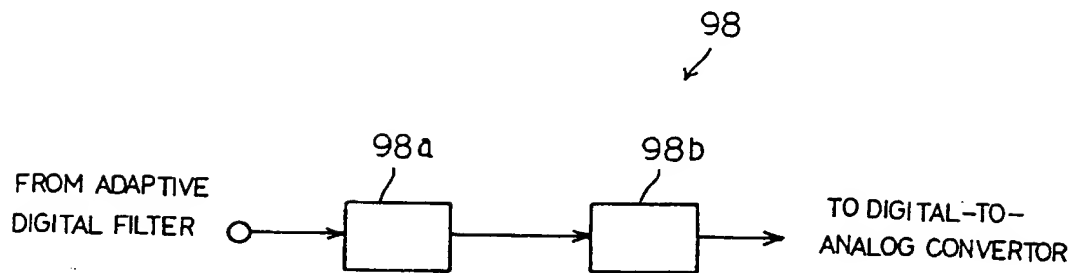


Fig. 13

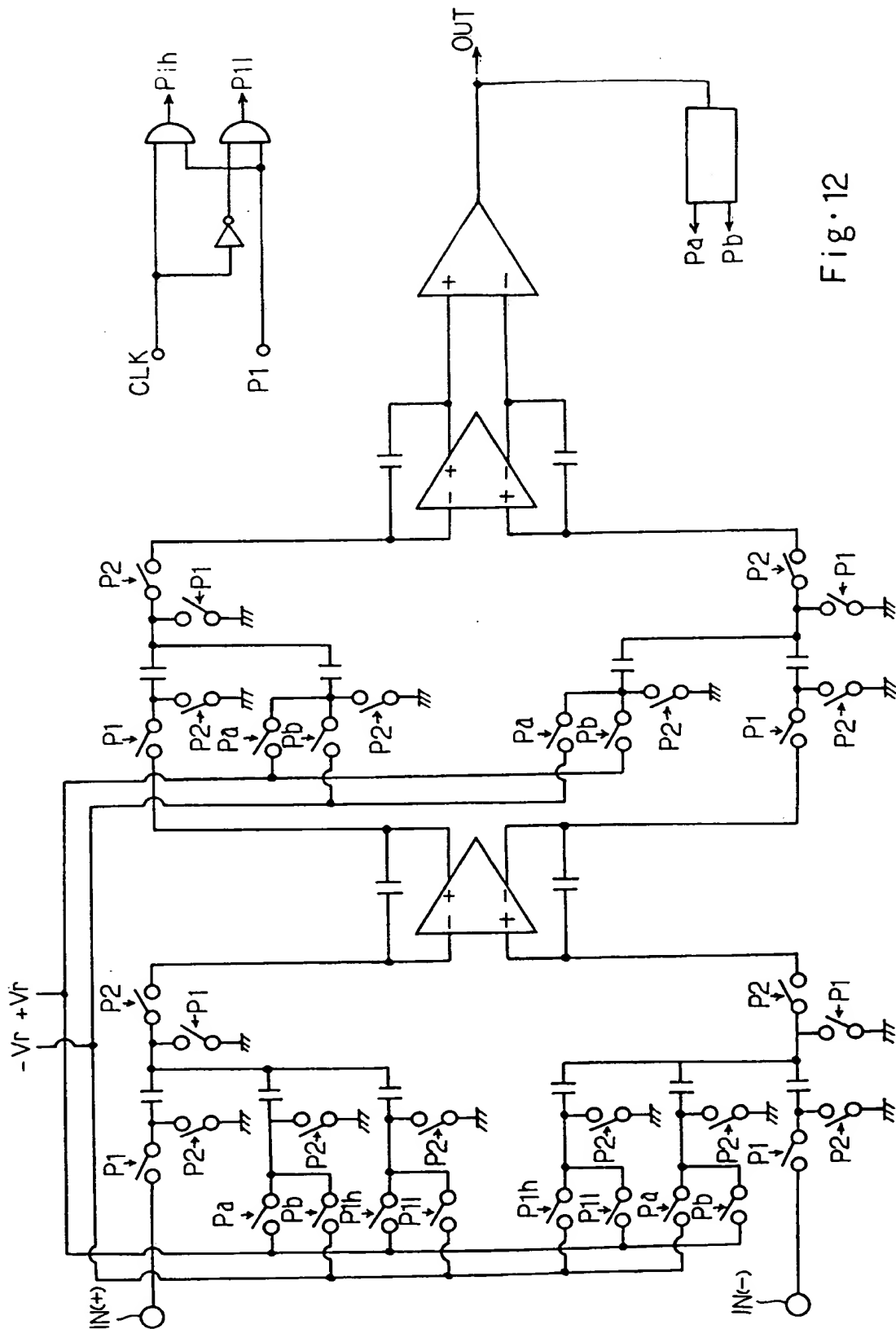


Fig. 12

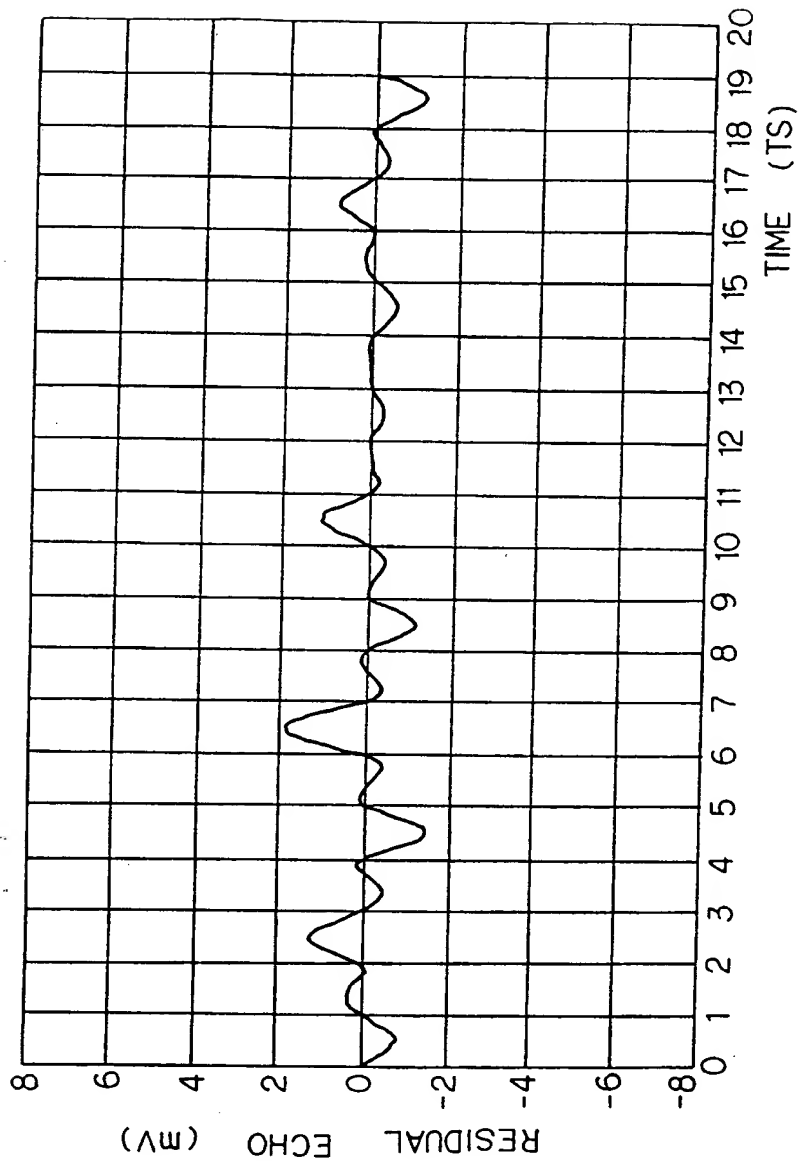


Fig.14A

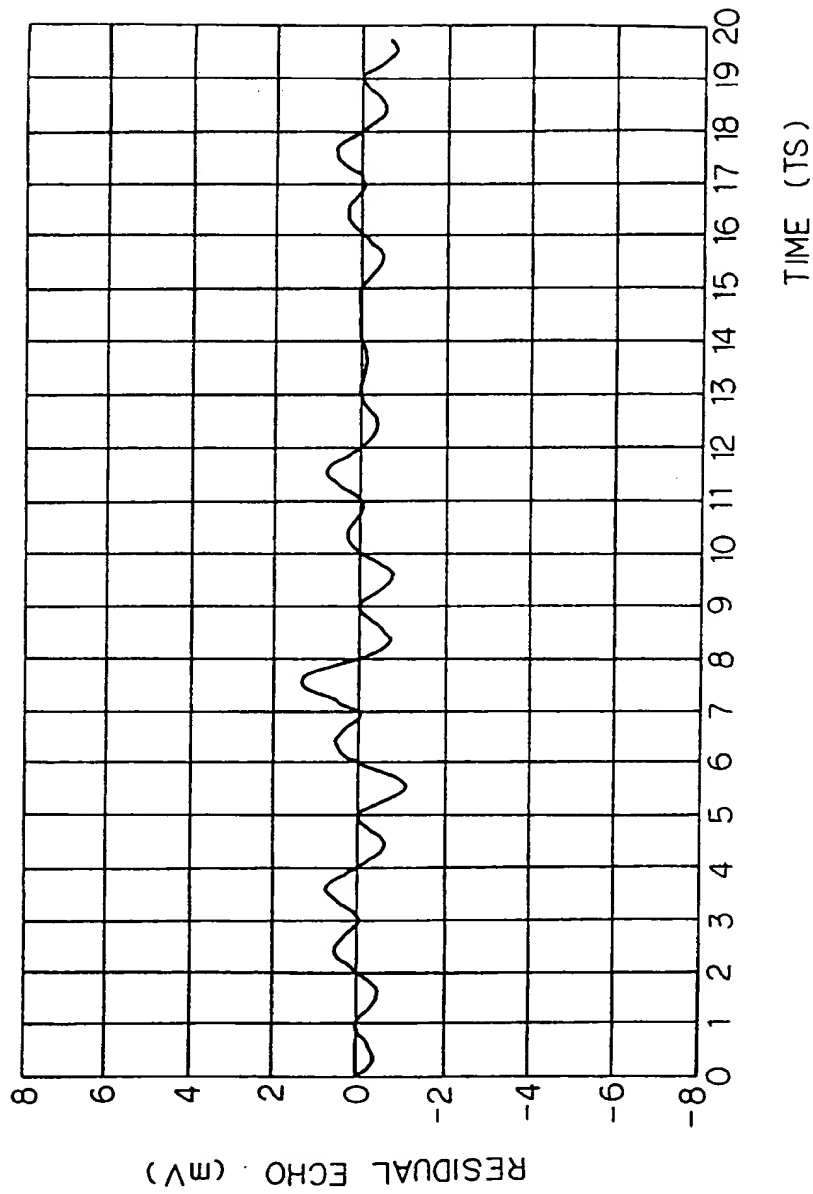


Fig. 14B

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EUROPEAN PATENT APPLICATION

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⑤ Int. Cl.⁵: **H04B 3/20**

②② Date of filing: 20.06.91

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④3 Date of publication of application:
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12.02.92 Bulletin 92/07

⑦① Applicant: **NEC CORPORATION**

54 Echo canceler having adaptive digital filter unit associated with delta-sigma modulation circuit.

57) An echo canceler comprises an adaptive digital filter circuit (42) for producing an echo replica signal on the basis of a transmit digital signal (TD) and a first digital signal indicative of a far-end signal, and an adder (45) for eliminating the echo signal from a received signal with reference to the echo replica

signal, wherein the echo replica signal is modulated by a delta-sigma modulation circuit (43) and, thereafter, converted into an analog signal for allowing the adder to operate on the echo replica signal and the received signal both in an analog form so that the adder with a narrow dynamic range can be available.

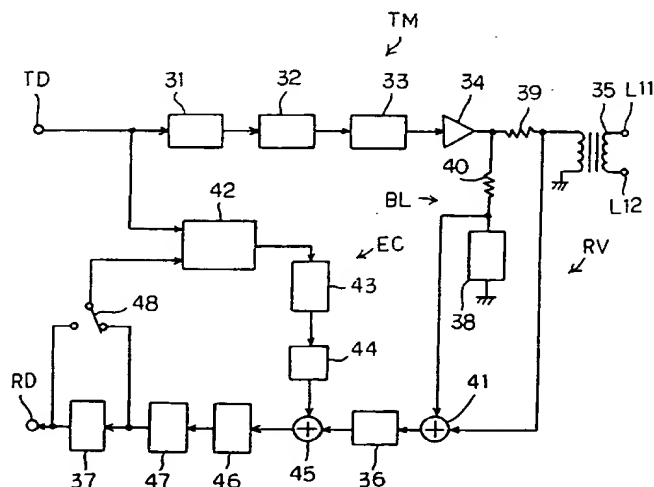


Fig. 3



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

| DOCUMENTS CONSIDERED TO BE RELEVANT | | | EP 91110190.5 |
|---|---|--|---|
| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
| A | FREQUENZ, vol. 37, no. 6, 1983, Schiele & Schön, Berlin Reinhard Till, " Adoptive Sprecherecho-Kompensation in Modems für die Duplex-Datenübertragung im Fernsprechnetz" pages 145-154 * Fig. 9 * | 1 | H 04 B 3/23 H 04 B 3/20 H 03 M 3/02 |
| D, A | IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, 36th ISSCC, February 1989, Technical Digest, New York, Haideh Khorramabadi et al. "An ANSI Standard ISDN Transceiver Chip Sed", pages 256,257 * Fig. 1; page 256, right column, lines 7-10 * | 1 | |
| A | US - A - 4 785 445 (GUIDOUX) * Fig. 1 * | 1 | TECHNICAL FIELDS SEARCHED (Int. Cl.5) |
| A | US - A - 4 769 808 (KANEMASA) * Fig. 8; abstract * | 1 | H 04 B H 03 M |
| The present search report has been drawn up for all claims | | | |
| Place of search | | Date of completion of the search | Examiner |
| VIENNA | | 09-12-1991 | DRÖSCHER |
| CATEGORY OF CITED DOCUMENTS | | | |
| X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document | | T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document | |

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